Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. A multilayer chip varistor, comprising:

a varistor body including a plurality of varistor layers and inner electrodes arranged to sandwich each of the varistor layers;

terminal electrodes formed on ends of the varistor body and connected to the inner electrodes; and

a glass layer formed between the varistor body and the terminal electrode, wherein,

the terminal electrode contains silver or an alloy whose principal component is silver which has a crystal structure of face-centered cubic lattice, and the inner electrodes contain palladium, platinum or an alloy whose principal component is palladium or platinum which has a crystal structure of face-centered cubic lattice; and wherein,

the terminal electrode further contains a glass material.

2. (Original) The multilayer chip varistor according to claim 1, wherein, in a cross section taken along a line passing through a center of the terminal electrode in a width direction thereof, each of the glass layers is formed to cover not less than 10% of a total length of an area which is covered with the terminal electrode, in the varistor body.

3. (Original) The multilayer chip varistor according to claim 1, wherein each of the glass layers has a thickness of 0.1 μm or larger.

4. (Original) The multilayer chip varistor according to claim 1,

wherein the terminal electrodes are formed by baking conductive paste containing a glass material, and

the glass layers are formed by the glass material melting from the conductive paste while baking the conductive paste.

5. (Original) The multilayer chip varistor according to claim 4, wherein the conductive paste contains metal and the glass material, and a content of the glass material is between 2 and 15 wt% with respect to an entire mass of the metal and the glass material.

6. (Canceled)

7. (Original) The multilayer chip varistor according to claim 1,

wherein the inner electrodes protrude from the varistor body into the terminal electrodes, and

at least root portions of the inner electrodes protruding into the terminal electrodes are covered with the glass layer.

8. (Withdrawn) A method of manufacturing a multilayer chip varistor, comprising the steps of:

forming a varistor body including a plurality of varistor layers and inner electrodes arranged to sandwich each of the varistor layers;

applying conductive paste containing a glass material onto ends of the varistor body; and

baking the applied conductive paste to form terminal electrodes and to form glass layers between the varistor body and the terminal electrodes by melting the glass material contained in the conductive paste.

9. (Withdrawn) The manufacturing method of a multilayer chip varistor according to claim 8, wherein, in a cross section taken along a line passing through a center of the terminal electrode in a width direction thereof, each of the glass layers is formed to cover not less than 10% of a total length of an area which is covered with the terminal electrode, in the varistor body.

10. (Withdrawn) The manufacturing method of a multilayer chip varistor according to claim 8, wherein each of the glass layer is formed to have a thickness of 0.1 μm or larger.

11. (Withdrawn) The manufacturing method of a multilayer chip varistor according to claim 8, wherein the conductive paste is baked at a temperature at least 70 degrees centigrade higher than a softening point of the glass material.

12. (Withdrawn) The manufacturing method of a multilayer chip varistor according to claim 8, wherein the conductive paste is baked at 700 degrees centigrade or higher.